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14EVE421

Fourth Semester M.Tech. Degree Examination, June/July 2017
Advances in VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain with necessary graph, the MOS enhancement and depletion mode to static plots. **(08 Marks)**

b. Explain with figure the basic operation of a MODFET. **(12 Marks)**

2 a. Bring out the salient features of CMOS and BiCMOS logic gates explain the operation of a 2-input Bi-CMOS NAND gate with neat schematic diagram. **(10 Marks)**

b. Discuss the energy band diagram of MIS systems under thermal equilibrium and various bias voltages with necessary diagrams. **(10 Marks)**

3 a. Derive an expression for the threshold voltage of an MIS device and hence explain enhancement and depletion modes of operation. **(10 Marks)**

b. Draw and explain the high frequency small signal circuit model for a MOSFET and hence derive an expression for its cut off frequency. **(10 Marks)**

4 a. Calculate the minimum capacitance for an n-channel MIS capacitor. Assume that the capacitor is made from S_i-S_iO_2-Al material systems. Given $N_a = 5 \times 10^{16} cm^{-3}$, oxide thickness = d = 12nm, the insulator relative dielectric constant = 3.9 and the semiconductor relative dielectric constant is 11.8. Assume $n_i = 1 \times 10^{10} cm^{-3}$. **(10 Marks)**

b. What is constant electric field scaling? Show that the threshold voltage and drain current scale linearly with dimensions and voltage on constant field scaling. **(10 Marks)**

5 a. Calculate the cut off frequency of a MOSFET given the following data: L = 1μm, $\mu_n^1 = 1200 cm^2/V\text{-sec}$, Z = 10L, $V_T = 1.1V$ and $V_G = 5V$. **(05 Marks)**

b. Realize CMOS circuit implementation of a NOR gate. **(05 Marks)**

c. With suitable mathematical analysis describe the short channel effects as applied to MOS circuits. **(10 Marks)**

6 a. With the help of neat diagram, explain the operation of nano tube FET. **(10 Marks)**

b. Bring out the differences between molecular computing and biological computing. List the key advantages of material used for molecular computing. **(10 Marks)**

7 a. Design the nMOS function blocks of 2 variables for the logic AND, NAND, OR, NOR, XOR, XNOR. **(12 Marks)**

b. Show that if an exponentially increasing driving circuitry is scaled such that each FET drives an effective load of e = 2.72, the propagation delay is minimum. **(08 Marks)**

8 Write a short notes:

a. Molecular diode

b. Dynamic ratio less logic

c. Hierarchy

d. Programmable logic. **(20 Marks)**

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